Center Innovation Fund: JPL CIF

Electronics Modernization

Completed Technology Project (2012 - 2012)

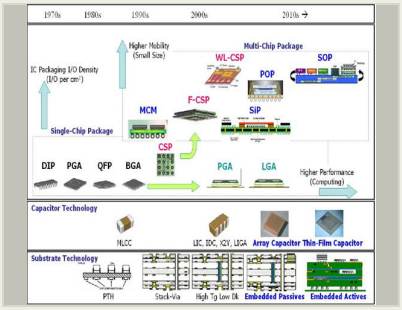
Project Introduction

There is a need to reduce mass and volume on any spacecraft whether for earth orbit insertion or travel within the solar system. Less mass and a smaller volume can dramatically reduce the cost of the launch vehicle as well as the spacecraft. Subsequently, the problem of too much mass and volume can be a result of the spacecraft structure, propulsion system, instrument and its electronics. This Workshop will focus on mass and volume reduction of the electronics.

Current electronic packaging designs used in our most recent spacecraft are comprised of technologies from the 1980's and 1990's. The current approach to electronic packaging design and selection uses well known design solutions because they are considered low risk and have space flight heritage; typically a ruggedized VME (Versatile Mechanical Euro) packaging architectures. Semiconductor features of this vintage utilize features that are measured in microns. As semiconductors have advanced, features are now measured in nanometers. We can use the example of the iPhone; with our current electronics design approaches the iPhone would be the size of a breadbox. These modern phones and devices such as laptop computers incorporate hundreds of new packaging technologies, some of which are appropriate for spaceflight and some that are not robust enough. The challenge is to identify the most useful technologies that are likely to survive rigorous spacecraft testing. With the exception of some earth-orbiting missions, virtually all other missions have unique environmental survival requirements. The primary objective of the Workshop will be to identify industry established state-of-the-art packaging technologies that can be leveraged without technology development with a focus on miniaturization. This will include active and passive components, substrates, connectors etc. Reliability and reworkability will be considered but will be a secondary objective in order to allow creativity. There will be a review of current JPL electronic packaging subsystems that can be exploited by reverse engineering the existing design. Also, new in-process JPL designs will be considered for redesign.

Anticipated Benefits

The results of the Workshop are broad and far reaching. This methodology can be a benefit to any spacecraft that has electronics. In most cases, funded missions after pre Phase A have selected an electronics architecture. There can be selected implementation of this methodology based on engineering decisions made as the design matures. Calculated mass savings on existing mission electronic subsystems for MSAP for a portion of the electronics went from .7 Kg to .3 Kg.



Project Image Electronics Modernization

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Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Center / Facility:

Jet Propulsion Laboratory (JPL)

Responsible Program:

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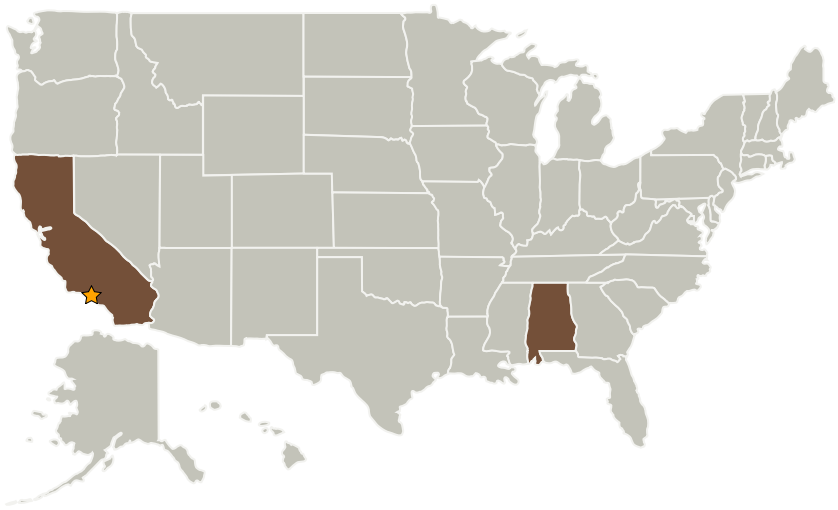
Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Type	Location
★Jet Propulsion Laboratory(JPL)	Lead Organization	NASA Center	Pasadena, California

Co-Funding Partners	Type	Location
Auburn University	Academia	Auburn, Alabama

Primary U.S. Work Locations	
Alabama	California

Project Management

Program Director:
Michael R Lapointe

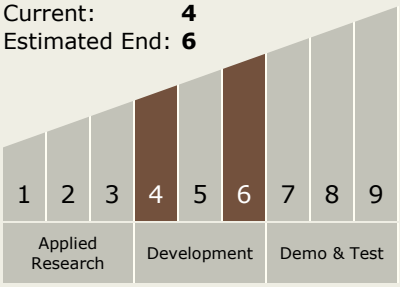
Program Manager:
Fred Y Hadaegh

Project Manager:
Jonas Zmuidzinas

Principal Investigator:
Donald V Schatzel

Technology Maturity (TRL)

Start: **4**
Current: **4**
Estimated End: **6**

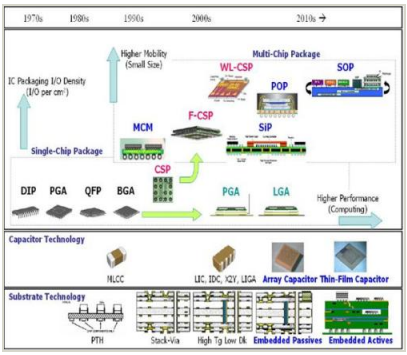


Technology Areas

Primary:

- TX02 Flight Computing and Avionics
  - TX02.1 Avionics Component Technologies
    - TX02.1.2 Electronic Packaging and Implementations

Images



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Project Image Electronics Modernization
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